# CMOS technology and integration of devices at KTH


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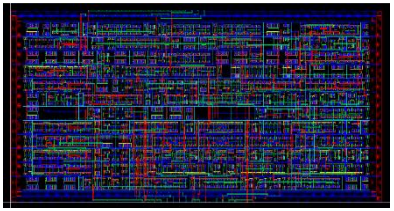
# CMOS process technology at KTH, why?

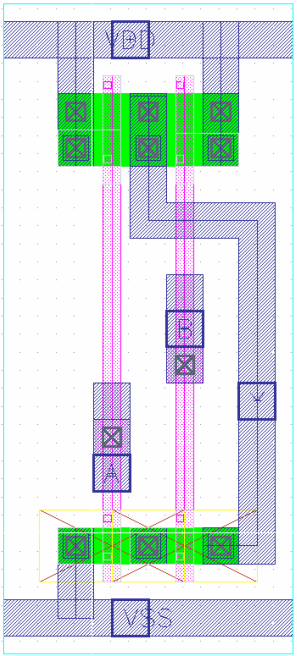
- Vision
  - Establish a CMOS process technology and design environment available to academic users
- Purpose
  - Benefit research projects where integration of circuits would add value

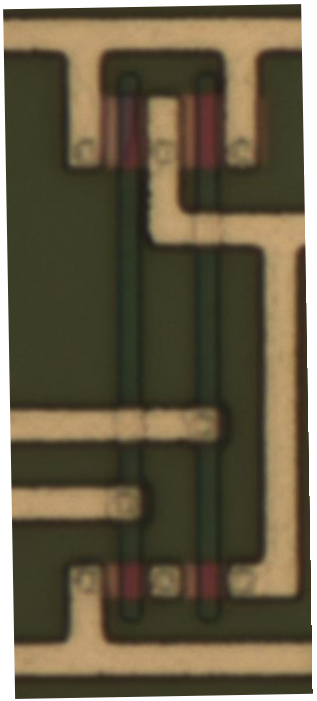
    *e.g. - Integration of new materials and devices with CMOS*
    *- Extended CMOS beyond conventional use cases*



- Current status
  - An FD SOI CMOS process (1P3M) with basic Process Design Kit has been established.
- Current objectives:
  - Demonstrate high yield (>80 %) on circuits containing more than 10 thousand transistors.
  - Extend the basic Process Design Kit with a larger standard cell library

# Design Rules



***I-line stepper, λ=365 nm***

Resolution: 0.5 µm, Alignment: 50 nm

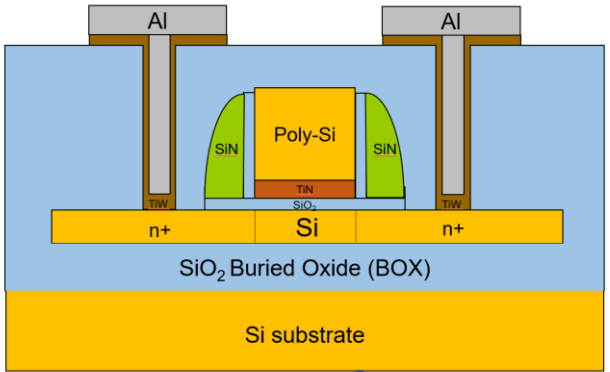
- Active area: width/open 2/2 µm
- Contact holes (CT): 1x1 µm$^2$
- M1, M2:  width/open 2/2 µm
- M1-CT: overlap 0.5 µm
- $L_G$ = 1 µm
- $W_{PFET}$=4 µm, $W_{NFET}$=2 µm

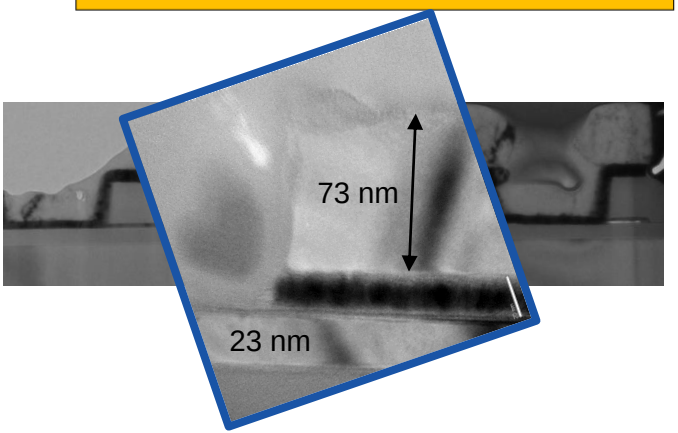
NAND: 16x36 µm$^2$

Die size of 7x7 mm : ~ 85 kNAND/die

*Die size of 21x21 mm : ~ 765 kNAND/die*

# Fully Depleted SOI CMOS




1. **Alignment mark**
2. **Si device layer litho , $t_{Si}$=25 nm**

*7 nm $SiO_2$ /18 nm TiN/100 nm $n^+$-poly-Si*

3. **Gate litho and etch**
4. **$n^+$ As impl. 9 keV, 1e15 $cm^{-2}$**
5. **$p^+$ $BF_2$ impl. 9keV, 1e15 $cm^{-2}$**

*ALD $SiO_2$/PECVD SiN spacers, RTA 1000 °C, 400 nm PECVD $SiO_2$*

6. **Contact hole litho**

*M1 DEP: 100 nm TiW/500 nm Al*

7. **Metal1 litho**

*RIE M1, Interlayer Dielectric Deposition 1 + CMP*

8. **VIA1 litho**

*RIE VIA1, M2 DEP: 100 nm TiW/500 nm Al*

9. **Metal2 litho**

*RIE M2, Interlayer Dielectric Deposition 2 + CMP*

10. **VIA2 litho**

*RIE VIA2, M3 DEP: 100 nm TiW/1000 nm Al*

11. **Metal3 litho**

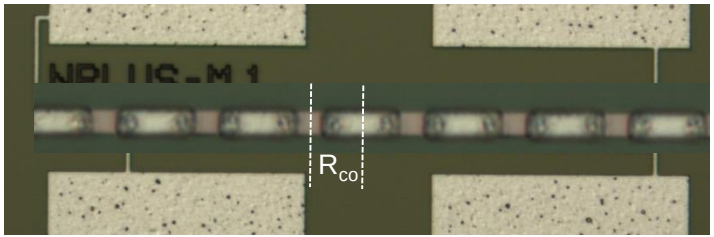
*RIE M3, PAD OXIDE Deposition*

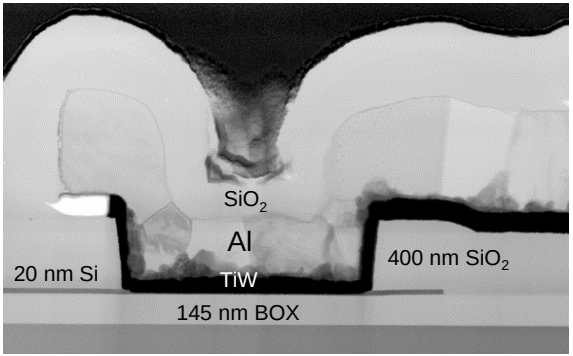
12. **OPEN PAD litho**

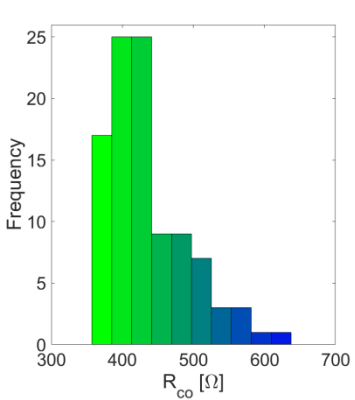
*RIE PAD OXIDE*

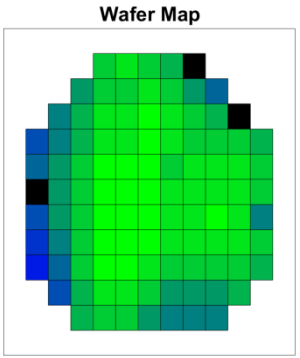
*10 % $H_2$/$N_2$, 400 °C anneal*

# Contact chains monitors



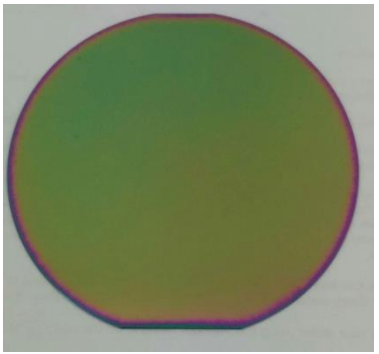



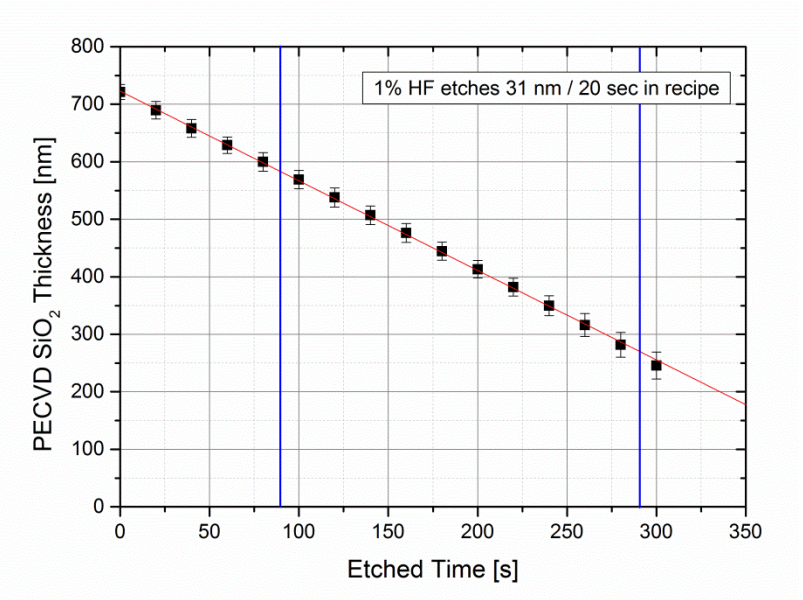



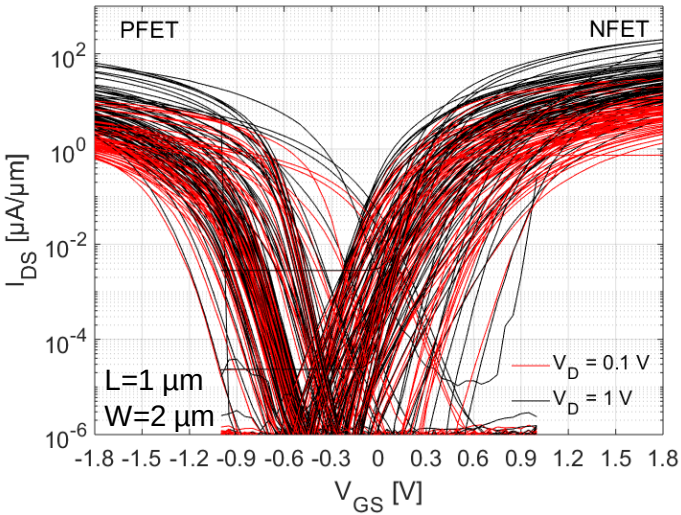

| Contact process development | Yield [%] |
|---|---|
| ETCH: RIE to ENDP<br>Resist strip: $O_2$ plasma<br>DEP: TiW/Al | < 1% |
| ETCH: RIE to or close to ENDP<br>Resist strip: $O_2$ plasma<br>CLEAN: 1 % HF<br>DEP: $Ar^+$ sputtering + TiW/Al | < 70% |
| ETCH: RIE on time<br>*1 nm < $t_{SiO2}$ < 40 nm left in CT hole*<br>Resist strip: $O_2$ plasma<br>CLEAN: 1 % HF 1 min<br>DEP: TiW/Al | > 95 % |

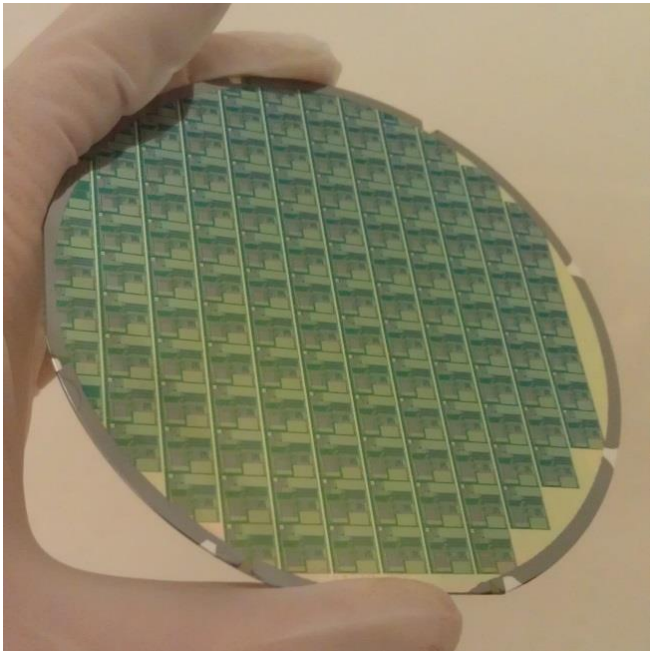
# HF Spray etching



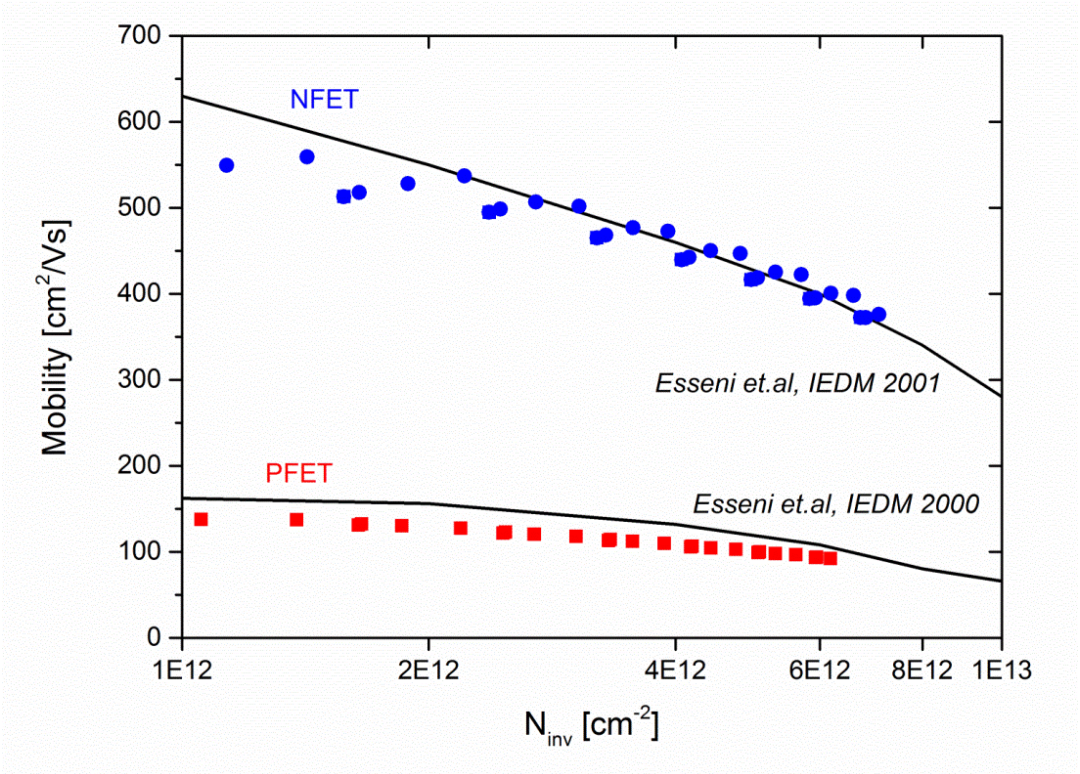


# Initial NFET and PFET electrical characteristics

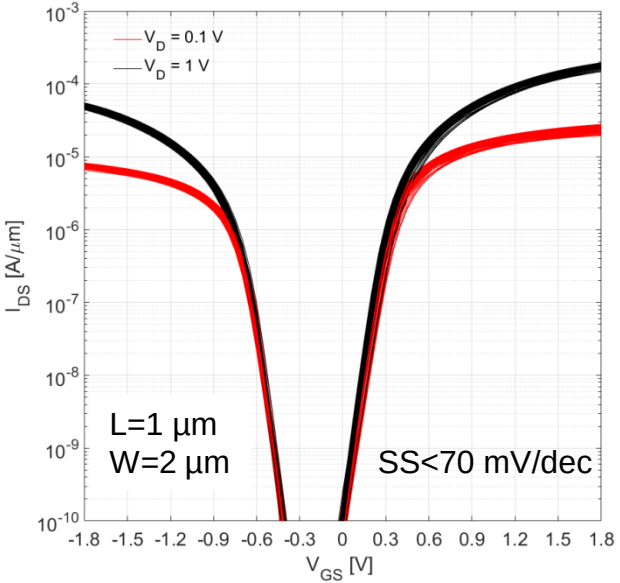


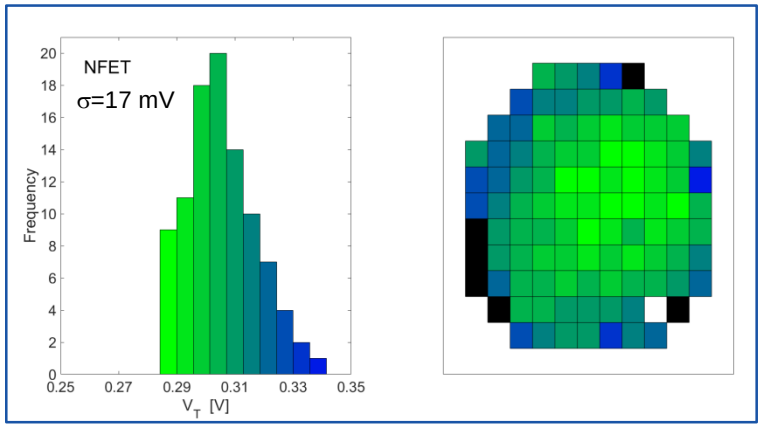



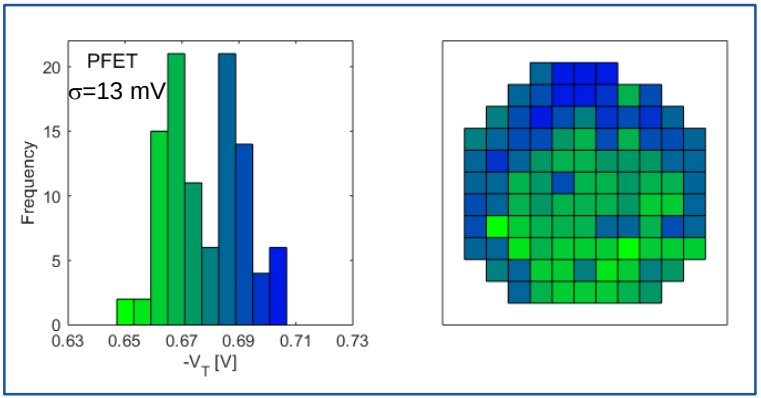
# Long channel mobility



# Device characteristics

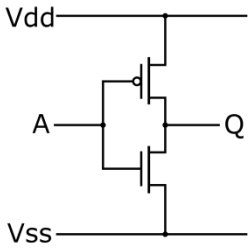


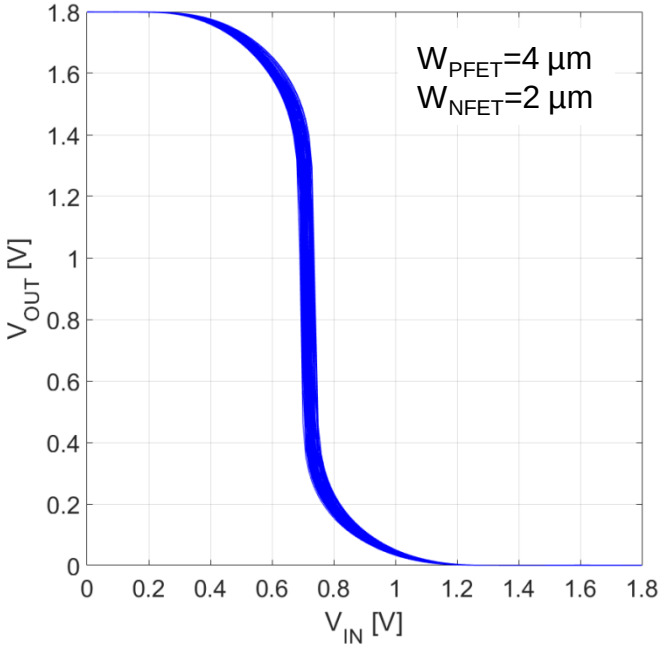



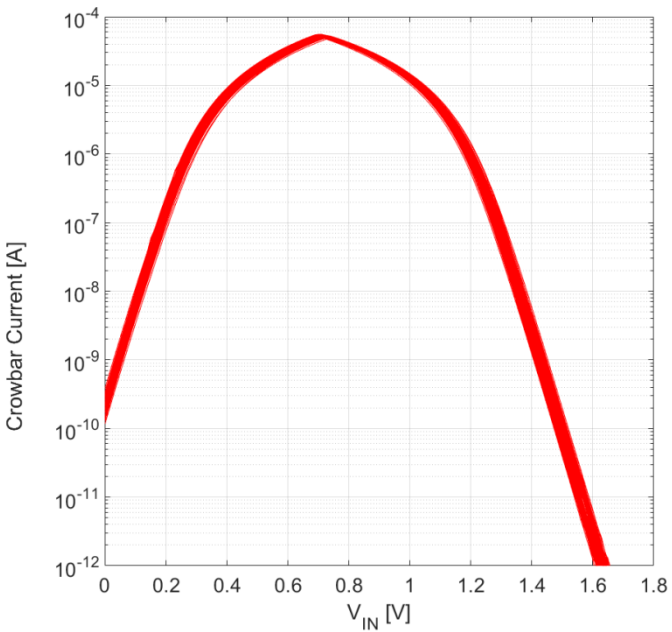




**Process Optimization**
Contact hole etch and Metal 1 dep
ALD TiN ($T_{dep}$ = 425 °C) as gate
RTA T=1000 °C, 60s

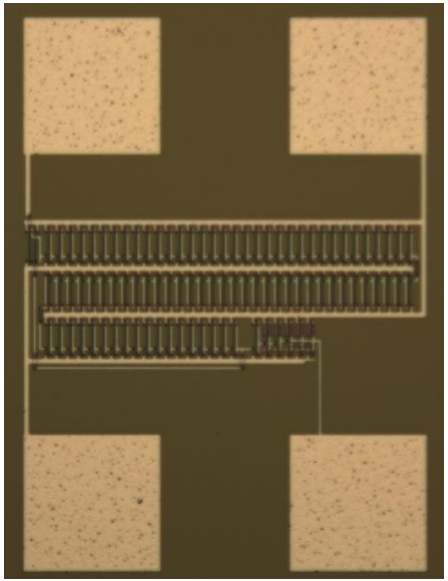
# Inverter

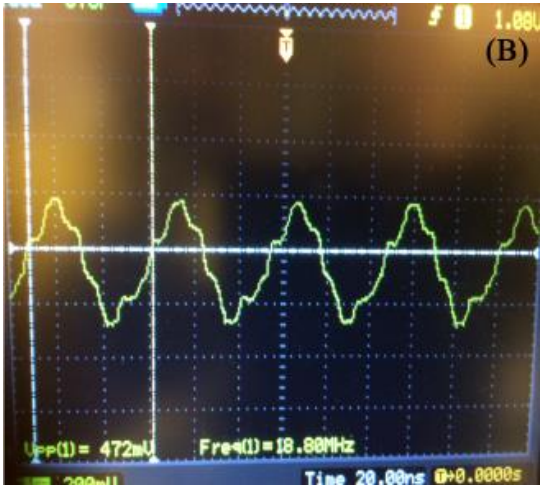

Vdd
A
Q
Vss


W_PFET=4 µm
W_NFET=2 µm
V_OUT [V]
V_IN [V]
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8


Crowbar Current [A]
V_IN [V]
10^-4
10^-5
10^-6
10^-7
10^-8
10^-9
10^-10
10^-11
10^-12
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8

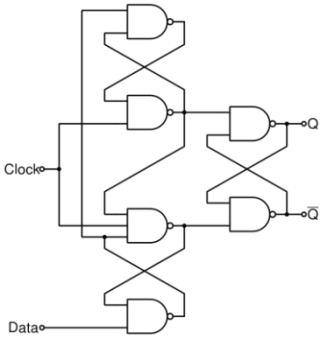
# 87 stage Ring Oscillator (176 FETs)

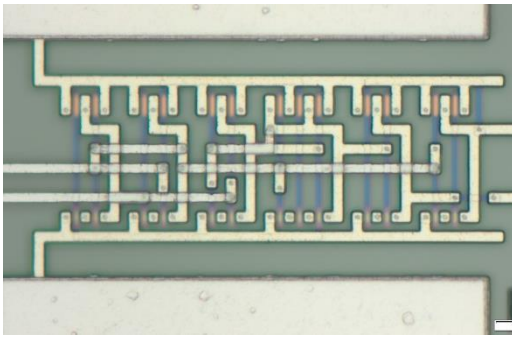


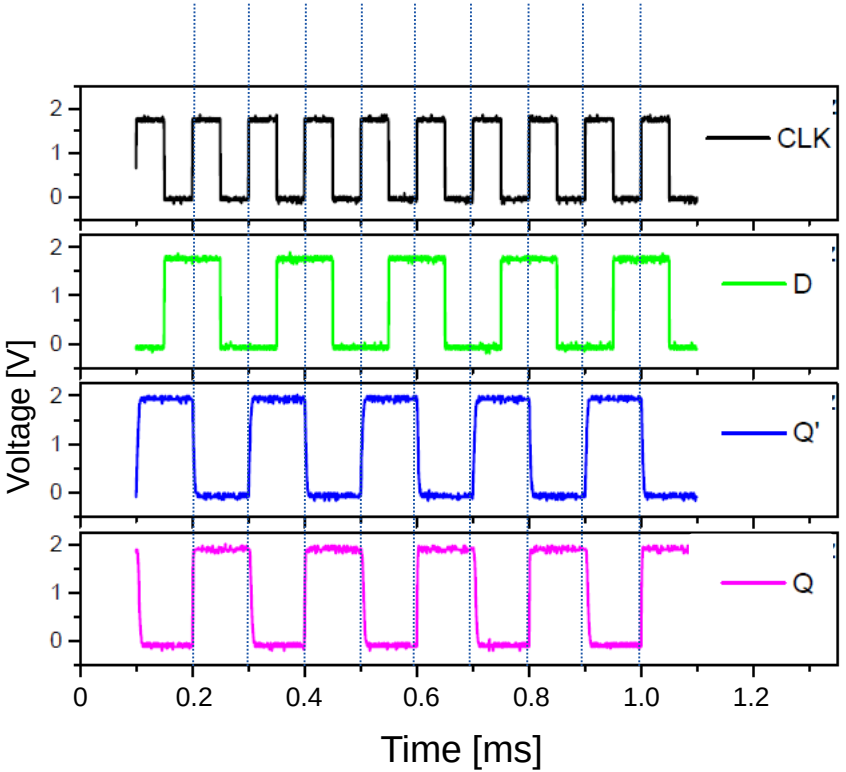



$$f_{RO} = 19\ MHz \rightarrow \tau = 305\ ps$$

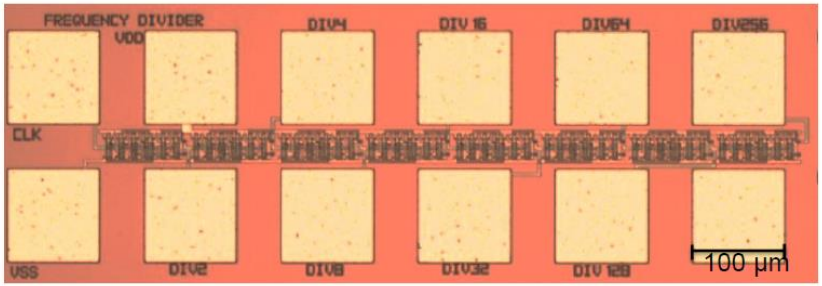
# D-Flip-Flop (26 FETs)

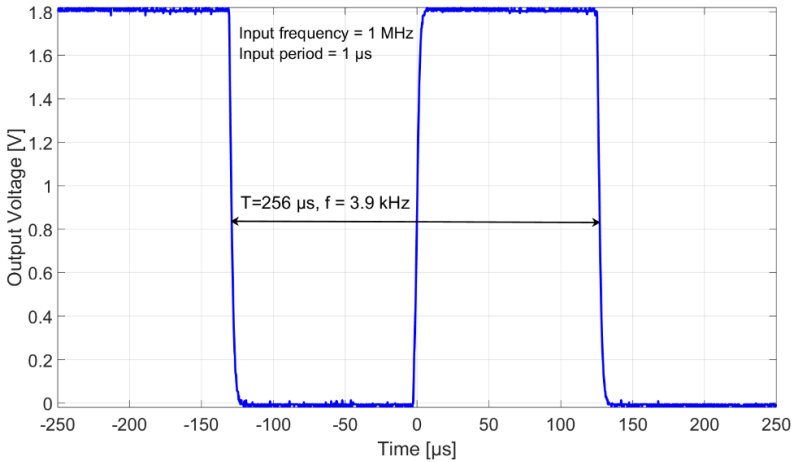




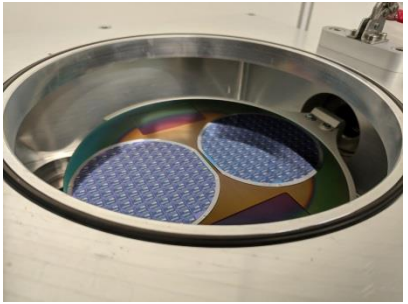
# Frequency divider (8 DFF, 212 FETs)

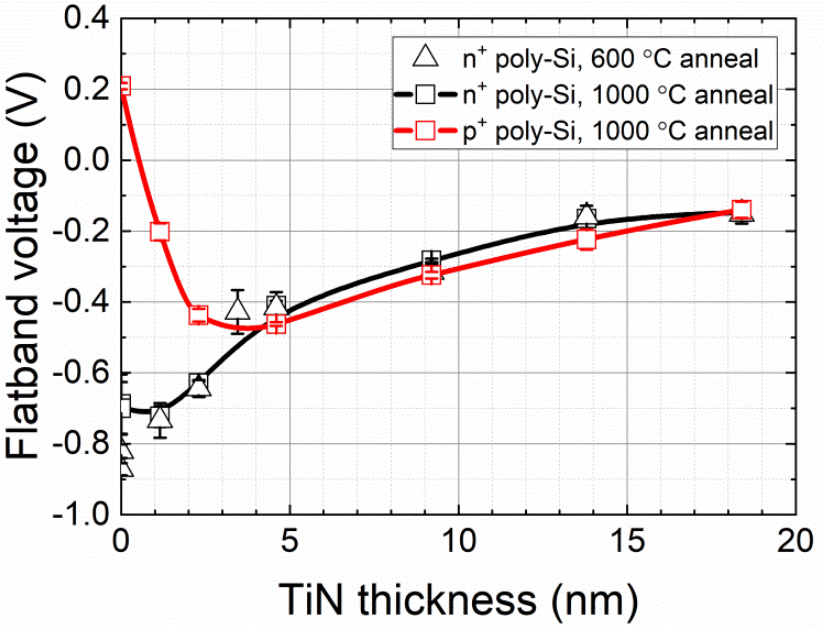



- Process with only 2 metal layers and $V_{Tp}$=-0.68 V & $V_{Tn}$=0.30 V (2019)

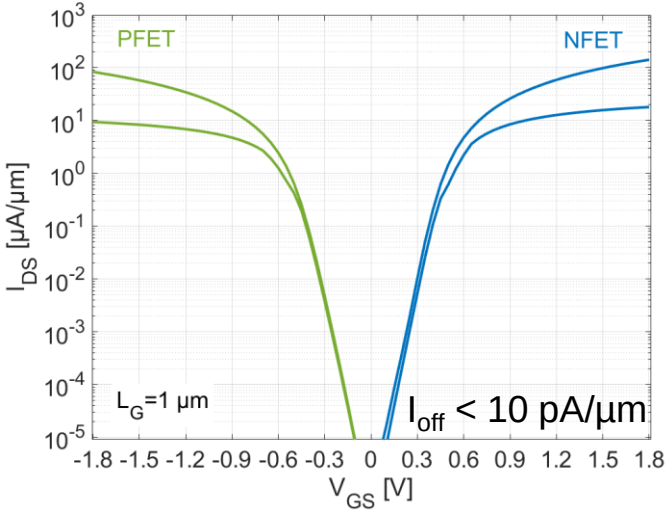
# ALD TiN, $TiCl_4$, $NH_3$, $T_{dep}$=425 °C

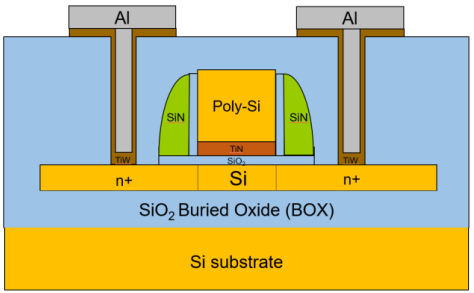



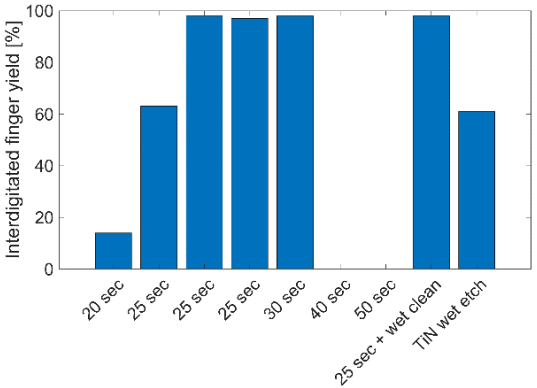


# 18 nm TiN enables symmetric $V_T$

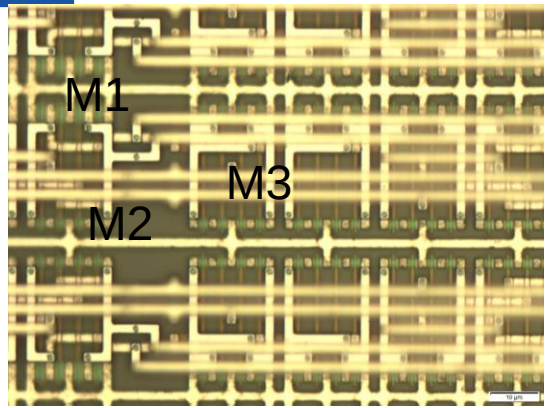
**Process Optimization**
Statistic Process Control ALD TiN
Gate oxide: 7.5 nm
RIE of poly-Si/TiN

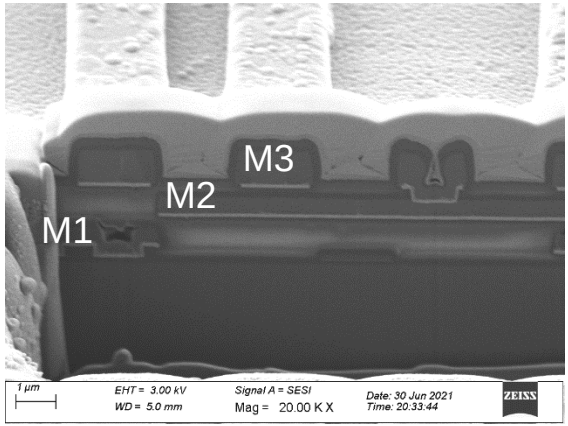


# 3 Level Metalization




1. **Alignment mark**
2. **Si device layer litho , $t_{Si}$=25 nm**

*7 nm $SiO_2$ /18 nm TiN/100 nm $n^+$-poly-Si*

3. **Gate litho and etch**
4. **$n^+$ As impl. 9 keV, 1e15 $cm^{-2}$**
5. **$p^+$ $BF_2$ impl. 9keV, 1e15 $cm^{-2}$**

*ALD $SiO_2$/PECVD SiN spacers, RTA 1000 °C, 400 nm PECVD $SiO_2$*

6. **Contact hole litho**

*M1 DEP: 100 nm TiW/500 nm Al*

7. **Metal1 litho**

*RIE M1, Interlayer Dielectric Deposition 1 + CMP*

8. **VIA1 litho**

*RIE VIA1, M2 DEP: 100 nm TiW/500 nm Al*

9. **Metal2 litho**

*RIE M2, Interlayer Dielectric Deposition 2 + CMP*

10. **VIA2 litho**

*RIE VIA2, M3 DEP: 100 nm TiW/1000 nm Al*

11. **Metal3 litho**

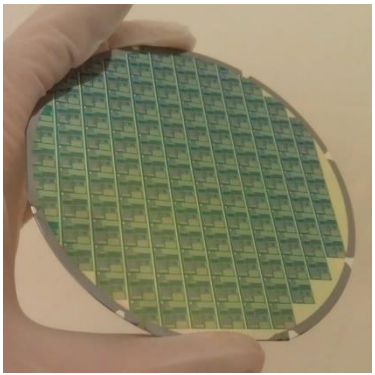
*RIE M3, PAD OXIDE Deposition*

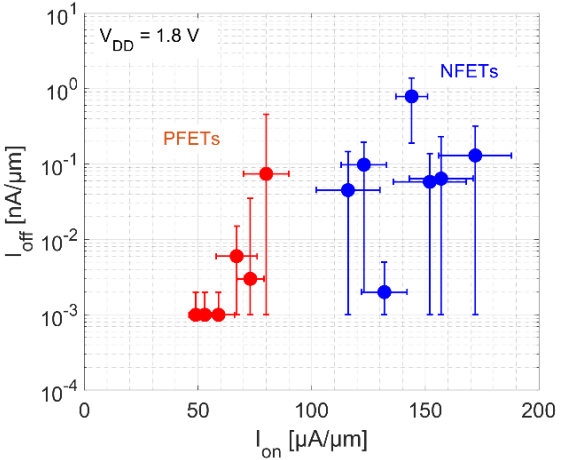
12. **OPEN PAD litho**

*RIE PAD OXIDE*

*10 % $H_2$/$N_2$, 400 °C anneal*

# KTH FDSOI CMOS performance

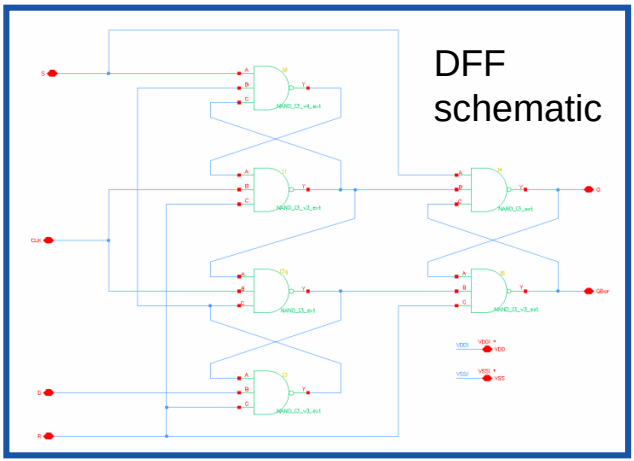





$I_{off}$-$I_{on}$ for the 7 fabricated wafers showing $I_{off}$<1 nA/µm and $I_{on}$ global variability of about ±10 % over a wafer. NFET $I_{on}$ is ~2x PFET $I_{on}$.

- An FDSOI CMOS process (1P3M) has been established
- $L_G$=1 µm, Supply voltage $V_{DD}$=1.8 V, Inverter propagation delay ~ 300 ps
- $I_{off}$< 10 pA/µm, PFET $I_{on}$=75 µA/µm, NFET $I_{on}$= 150 µA/µm.

# Process Design Kit

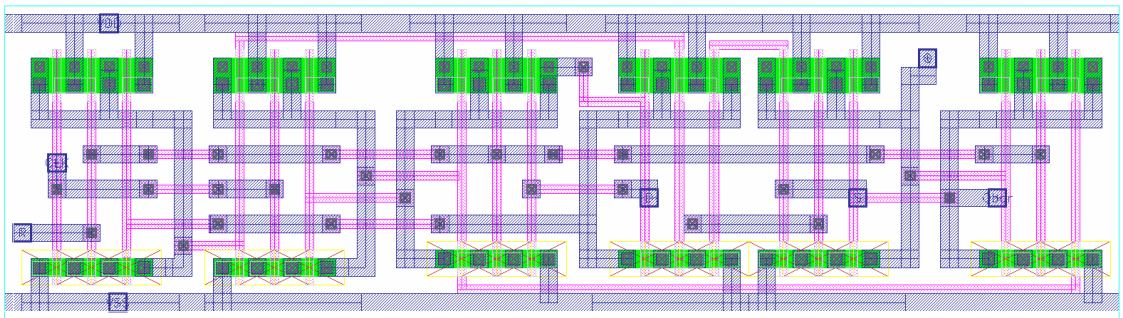



Design Rule Check (DRC)
Layout vs. Schematic (LVS)

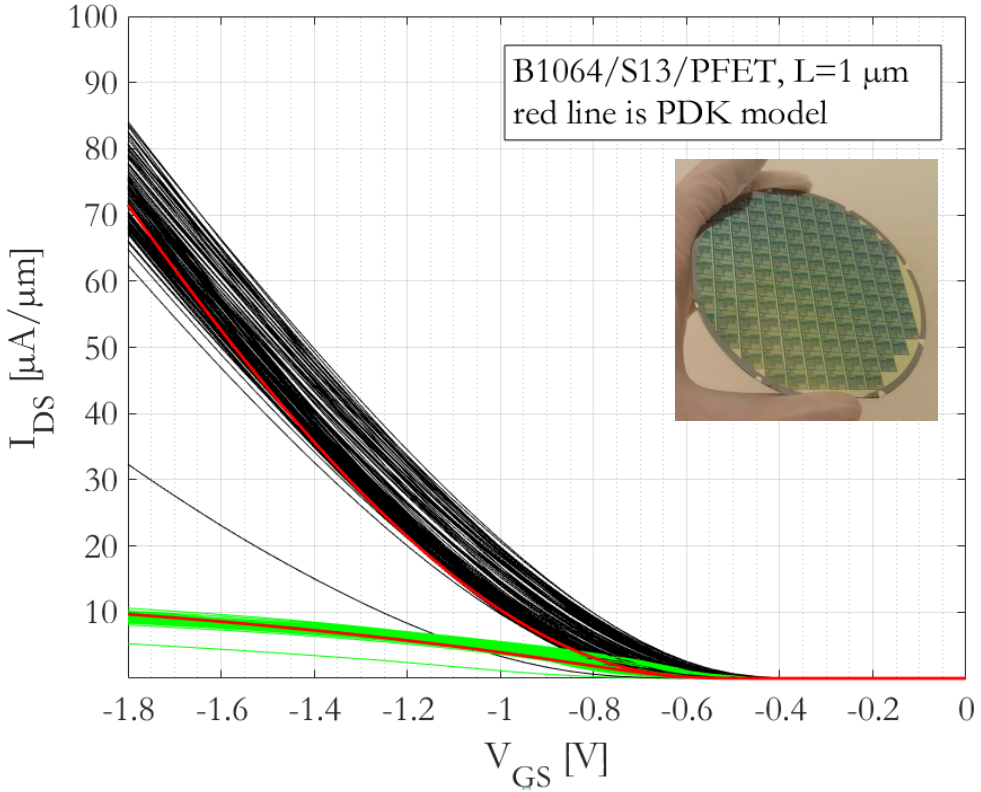
## Process Design Kit (KTH FD SOI)

- Design rules (layers, min width, min distance…)
- Parametrisized MOSFETs
- Calibrated transistor model (UTSOI from Leti)
- Post layout extraction of parasitic R,C
- Standard cell library, timing data
- Automatic Place and Route digital cells

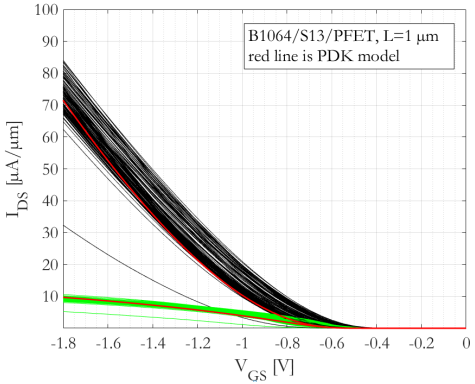
DFF
layout

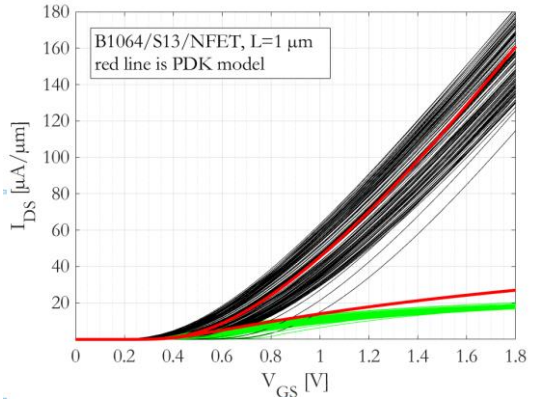


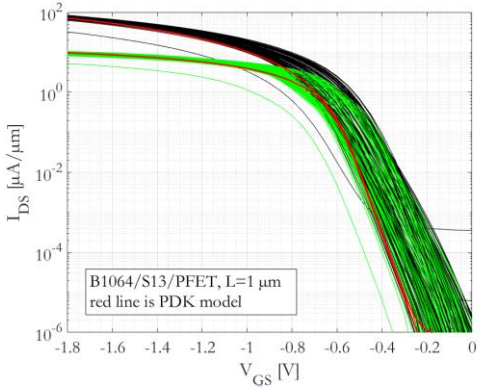
# Calibrated UTSOI model in PDK and global variability

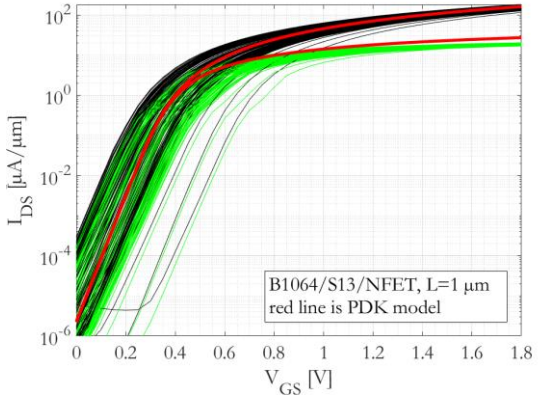


# Calibrated UTSOI model in PDK and global variability

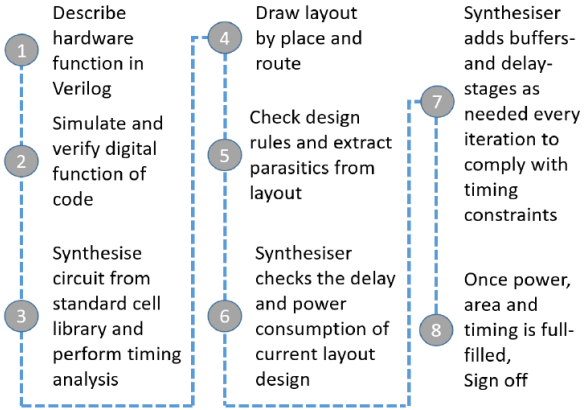


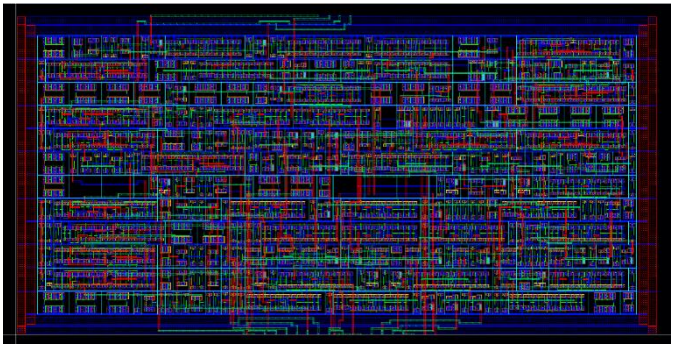



# Digital Design Flow (RTL to GDSII)




3. Standard cell library, timing data
4. Automatic Place and Route digital cells
5. Post layout extraction of parasitic R,C



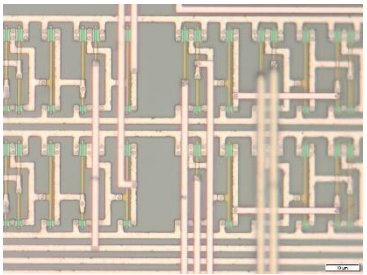
A Serial Peripheral Interface (SPI) designed using Verilog A code and implemented using KTH PDK Cadence tools:

```
GENUS211 (digital synthesis)
INNOVUS181 (digital place & route)
XCELIUM1803  (digital simulation)
IC618 (Virtuoso Schematic and layout editor)
PVS161 (DRC & LVS physical verification)
```

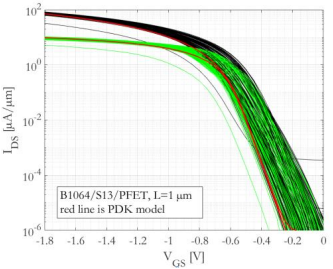
# Summary KTH FDSOI CMOS

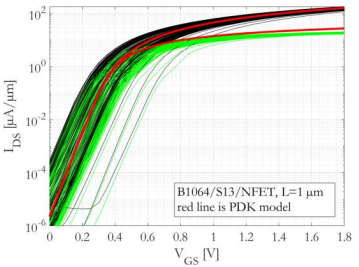
Saul Rodriguez Duenas, Mattias Ekström, Per-Erik Hellström

## 3 Metal Layer Interconnects

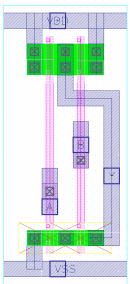


## Calibrated FD SOI Model




## Digital Standard Cell Library



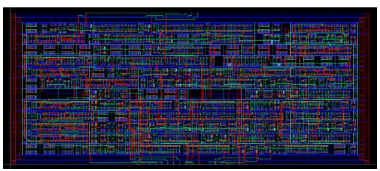
Die size of 7x7 mm : ~ 85 kNAND/die

Max frequency ~ 10s of MHz

## Digital Design Flow: Verilog RTL to layout

```
GENUS211 (digital synthesis)
INNOVUS181 (digital place & route)
XCELIUM1803  (digital simulation)
IC618 (Virtuoso Schematic and layout editor)
PVS161 (DRC & LVS physical verification)
```

cadence® ACADEMIC NETWORK



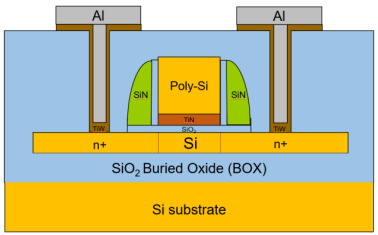
# KTH FDSOI CMOS: Current developments

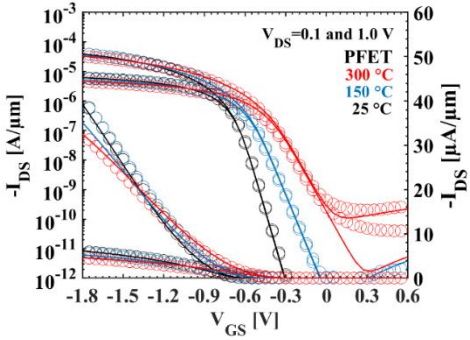
- **Second version of PDK (to be completed Q3 2022)**
  - Re-design standard cells to increase yield.
  - Extend the cell library for the digital design flow.
  - New maskset with goal to achieve high yield on circuits >10 kTransistors.

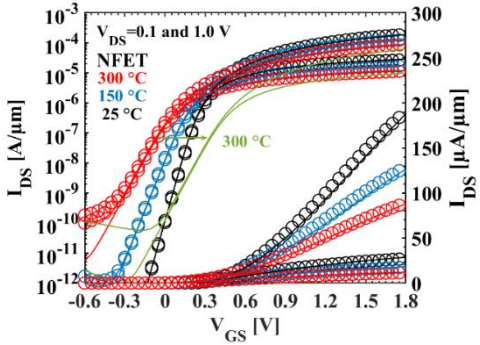
- **Develop and integrate analog components in FDSOI Process**
  - High sheet resistance resistor
  - Metal-Insulator-Metal Capacitor

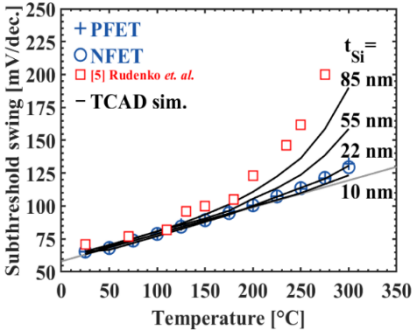
- **Extend KTH FDSOI CMOS webpage**
  - https://www.kth.se/profile/pereh/page/cmos-technology-for-academia

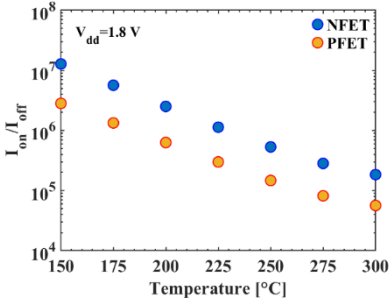
# High (>200 °C) temperature operation

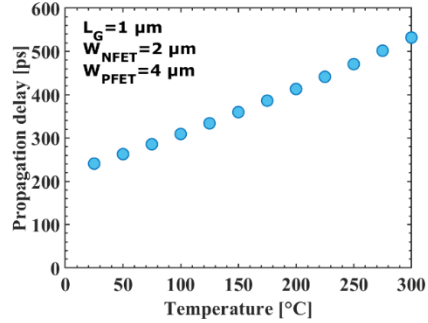


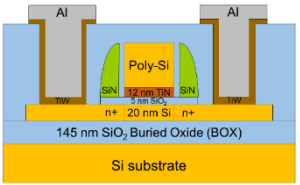



# Potential use cases




Transparent electronics

High process temperature
> 400 °C, 3D integration

High operating temperature
> 175 °C

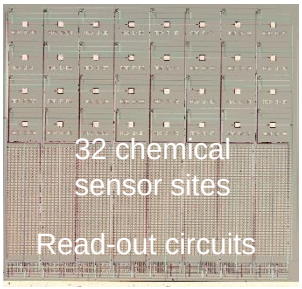
Digital Design Flow
Standard cells, place and route, parasitic extraction and timing analysis.

FDSOI CMOS
VDD=1.8 V
$\tau$=250 ps, ft=4 GHz

co-integration of new materials:
Graphene, 2D, Ge, piezo, photonic, ferroelectric

Analog Design Environment
Resistor, Capacitor, I/O devices
High Voltage (>2.5 V) CMOS

High Frequency Transistors
> 100 GHz




- **Mature**, ready to be used in projects
- **Proof of concept** is demonstrated. Clear development path exist
- **Promising idea** but technological barriers exists, potentially solved in a research projects

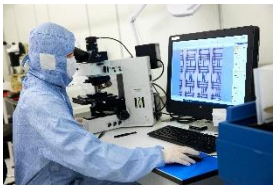
# Thanks for your attention!

Assoc Prof.
Per-Erik Hellström

Assoc Prof.
Saul Rodriguez Duenas

Dr.
Mattias Ekström

Students at Master and PhD level are acknowledge for contributions to KTH CMOS Technology



Vetenskapsrådet

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